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High Performance and Power Efficient Comparator Using Scalable Parallel Prefix Tree

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Abstract

A new comparator design featuring of wide-range and high-speed using only digital CMOS cells. The comparator exploits a novel scalable parallel prefix tree structure that allows the comparison outcome of most significant bit, towards least significant bit when compared bits compared bits are equal .This method reduces dynamic power dissipation by eliminating unnecessary transitions. And a comparator with maximum fan-in and fan-out of five and four respectively. The main advantages of this design are high speed and power efficient. Additionally this design uses a regular reconfigurable VLSI topology that allows input and output as a function of bit width. Simulation for 16-b comparator shows a total power consumption of 27mW using TSMC technology.

Keywords: High-speed wide bit comparator architecture, parallel prefix tree structure

Introduction

COMPARATORS are main design elements for wide range of applications-scientific computations (graphic signal processing)[1]. The prefix tree structure's area and power consumption can be improved by two-input multiplexer instead of 2-b comparator cells at each level for the evaluation [2]. In this level requires many stages for the comparison of bit width of 16 bits , but suffers high power consumption due to every cell in the structure being active and again the structure perform only "greater-than" or "less-than" comparison not equality

To improve speed and reduce power consumption, design depends on pipelining [3] and power down mechanism [6]. A 16-b comparator requires many pipeline cycles using multiphase clocking scheme [7].

A multiplexer based structure to split 16 bit into two stages, the first stage output maybe input of a second stage [4], here require of two phase domino clocking [5], and thus limits operating speed.

To reduce the drawback of previous designs (such as high power consumption, multi cycle computation, Custom structures unsuitable for continued technology)

Here we use of standard CMOS cells to achieve High speed, scalable, wide range, power efficient. And also following features

1. It's a reconfigurable arithmetic algorithms , with input and output are fully custom and standard cell approaches , so achieve easy to market
2. A novel MSB to LSB parallel prefix tree structures reduces switching activity, parallelism in each level to improve speed

CMOS cells with maximum fan-in and fan-out of 5 & 4 respectively, regardless of the comparator bit width. So make it easy to characterize

Architectural Review of Comparator

It contains comparison resolution module is a novel MSB-to-LSB parallel prefix tree structure that performs bit wise comparison of 2 N-bit operands A and B, denoted as $A_{n-1,}A_{n-2,,,}A_0$ and $B_{n-1,}$ $B_{n-2,,,}$ B0 , that ranges from N-1 for MSB to 0 for LSB. That performs bitwise comparison asynchronously from left to right; comparison logic's computation is triggered only if all bits of greater significance are equal.

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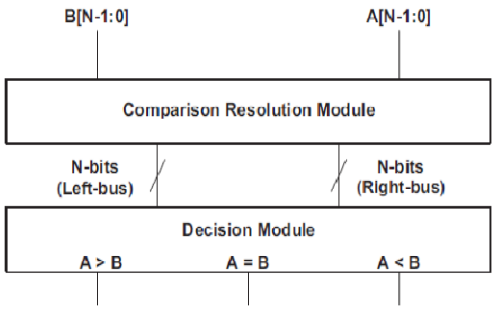

Fig 1: Block diagram of comparator

The parallel structure encodes the result into two N bit buses, the left bus and the right bus, comparison result as each bit position evaluated, such that

$$\begin{cases} \text{if } A_k > B_k, & \text{then } \text{left}_k = 1 \text{ and } \text{right}_k = 0 \\ \text{if } A_k < B_k, & \text{then } \text{left}_k = 0 \text{ and } \text{right}_k = 1 \\ \text{if } A_k = B_k, & \text{then } \text{left}_k = 0 \text{ and } \text{right}_k = 0. \end{cases}$$

To reduce switching activities, the bitwise comparison of every bit of lower significance is terminated and all such positions are set to zero both buses. Thus, there is never more than one high bit on either bus.

The decision module uses two OR-networks to output of the final comparison based on OR scans of all of the the bits on the left bus and all of the bits on the right bus. If LR= 00 then A=B, if LR= 10 then A>B, if LR= 10 then A<B, and LR= 11 not possible.

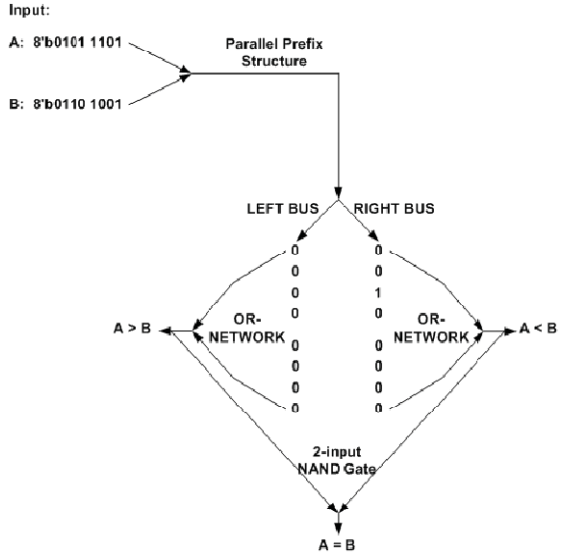

Fig 2: Comparison example of 8-b

An 8-b comparison of input A= 01011101 and B= 01101001 is shown in Fig 2. A parallel prefix tree structures generates the encoded data on the left bus and right bus for each pair of corresponding bits from A and B. Here $A_7 = 0$ and $B_7 = 0$ encodes as $\text{left}_7 = \text{right}_7 = 0$, $A_6 = 1$, and $B_6 = 1$ encodes as $\text{left}_6 = \text{right}_6 = 0$, and $A_5 = 0$ and $B_5 = 1$ encodes as $\text{left}_5 = 0$ $\text{right}_5 = 1$. Since the bits are unequal, the comparison terminates and a final comparison decision can be based on first three bits evaluation. Then the OR-networks perform the bus OR-scans, resulting in 0 and 1.

Design of Comparator

Comparator design based on novel scalable parallel scalable prefix tree that contain 5 sets, each set produces outputs that serve as inputs to the next set[exception of set 1]

Set1 compares A and B, using of Ψ type cells. Ψ type cells provide termination flag D_k to Sets 2 and 4.

$$\Psi: D_k = A_k \oplus B_k$$

Set 2 consist of $\sum_2$- type cells, which combine the termination result of set 1 using NOR logic to limit fan in and fan out to a maximum of four.

$$\sum_2 : C_{2,m} = \text{COMP}\left(\sum_{i=4m}^{4m+3} D_i\right).$$

Set 3 consists of $\sum_3$ type cells , which are similar to $\sum_2$- type cells . A $\sum_3$cell not comparison functionality purpose to limit fan-in and fan-out

$$\text{Levels}_{\text{set3}} = (\log_{16}(N)).$$

$$\sum_3 : c_{3,m} = \text{COMP}\left(\sum_{0}^{m} C_{2,i}\right)$$

From left to right, the first four $\sum_3$- type cells in set 3 combine the 4-b partition comparison outcomes from one, two, three, and four. 4-b partition of set 2.

Since fourth $\sum_3$- type cells has fan-in of 4, the number of levels in set 3 increases and set 3 with a fan-in of only 2 and fan-out of 1.

Set 4 consist of Ω- type cells, whose

Outputs controls the select inputs of Φ- type cell in set 5.

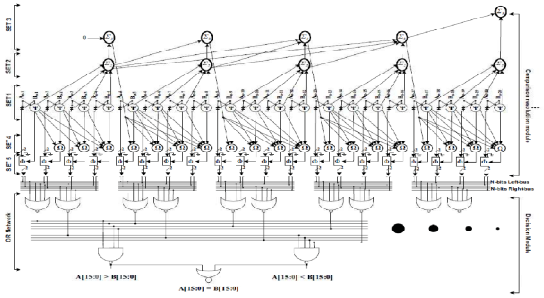

Fig 3: Comparison Module and Decision Module Implementation

Set 5 consist of Φ-type cells (2 input,2 bit wide multiplexer). One input is (A_k, B_k), and the select control input is based on the result of set 4. Where all left-bit codes and all right-bit codes from left bus and right-bus.

$$\Phi: F_k^{1,0} = Y_k \times M_k + \bar{y}_k \times (00)$$

The output $F_k^{1,0}$ denotes the ”greater-than”, “less-than” or “equal to” final comparison decision.

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Comparator Bitwidth	Transistor Count					
	Set 1	Set 2	Set 3	Set 4	Set 5	Total
16-b	16×2	4×8	31×3	16×4	15×7	326

Table 1: Total Number of Transistor for 16-b Comparator

Area, Speed, Power Calculation

A. Calculation of Area

Here calculate total number of cell counts.

B. Calculation of Operating Speed

Analyze the critical path delay of 16 bit input. The delay DCRM for the comparison resolution module is.

$D_{CRM} = D_{set1} + D_{set2} + D_{set3} + D_{set4} + D_{set5}$

C. Requirements of Power

Minimizing the switching activity reduces the average power dissipation is a important technique for low low power design. The total power consumption of 16 bit comparator is 27mW, and reduces power consumption up to 90% by using novel scalable parallel prefix tree.

Simulation-For Comparator

Input:
A= 1010000010111111
B= 1010000010111111
Output:
A=B(Equal)= 1

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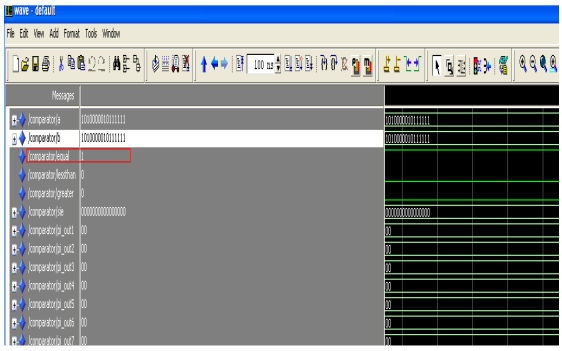

Fig 4:Output window for bit equal

When give input (A=B) means the equal line will increase from lower to higher. The remaining lines are still in lower level.

Input:
A= 1011000010111111
B= 0010000010111111
Output:
A > B= 1

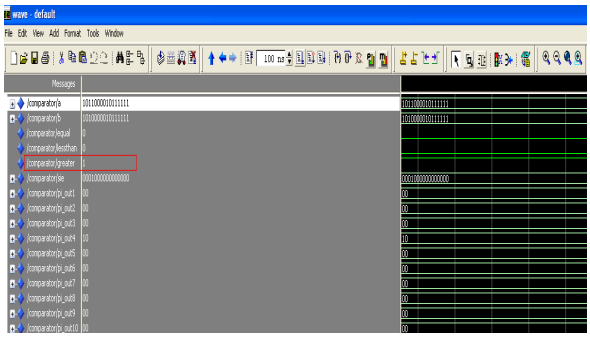

Fig 5: Output window for bit greater than

When give input (A>B) means the greater than line will increase from lower to higher. The remaining lines are going to lower level.

Input:
A= 0010000010111111
B= 1110000010111111
Output:
A<B=1

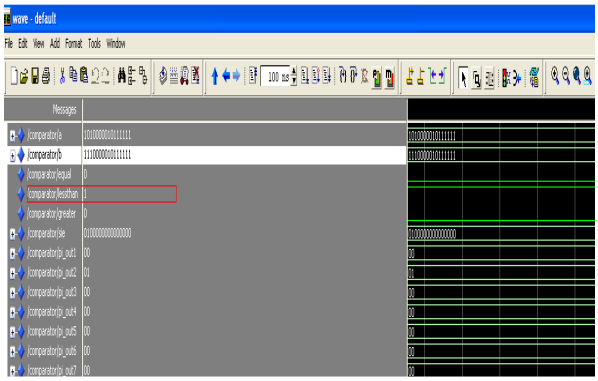

Fig 6:Output window for bit less than

When give input (A<B) means the less than line will increase from lower to higher. The remaining lines are going to lower level.

Conclusion

Here able to achieve high-speed and low-power comparator using regular digital hardware structures .This structures allows prediction of comparator characteristics for arbitrary bit widths

Parallel prefix tree structure is novel, it allows comparison from MSB to LSB, using parallel operation, rather than rippling. Here less than 35% transistor used in the design is active and also all cells are locally interconnected

FUTURE WORK: To reduce the power consumption and improve speed by adapting dynamic analog implementation for the comparator resolution module, zero detector for decision module.

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